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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/784,813	02/24/2004	Jane Lu	2946-D-Z	1174

7590 12/23/2005

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EXAMINER	
NORRIS, JEREMY C	

ART UNIT	PAPER NUMBER
2841	

DATE MAILED: 12/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

8/11

Office Action Summary	Application No.	Applicant(s)	
	10/784,813	LU ET AL.	
	Examiner	Art Unit	
	Jeremy C. Norris	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *11-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 28 October 2005 has been entered.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 11, 12, 15, and 16 are rejected under 35 U.S.C. 102(b) as being anticipated by US 5,509,200 (Frankeny).

Frankeny discloses, a thermally enhanced printed circuit (PC) wiring board to which ball grid integrated circuit packages (46) are to be mounted thereon comprising a relatively thin, conductive metal core layer (1) having oppositely facing surfaces and one or more holes (4) in the metal core at each of plurality of through-core via sites, first and second thin rigidifying non-conductive laminate sheet (6) attached to said oppositely facing surfaces, respectively, and least one conductive circuit pattern (12) on at least one of said thin rigidifying non-conductive sheets and a plurality of vias (8) thereon

[claim 11] including a plurality of vias (14) made by plating build-up and connecting to the core from both the top and bottom sides thereof [claim 12], including a plurality of vias (13, 14) selected from Type 1, Type 2, or Type 3 vias as defined herein [claims 15, 16].

Claims 11, 12, 15, and 16 are rejected under 35 U.S.C. 102(b) as being anticipated by US 5,640,761 (DiStefano).

DiStefano discloses, a thermally enhanced printed circuit (PC) wiring board to which ball grid integrated circuit packages are to be mounted thereon (see col. 1, lines 35-45) comprising a relatively thin, conductive metal core layer (30) having oppositely facing surfaces and one or more holes (58) in the metal core at each of plurality of through-core via sites, first and second thin rigidifying non-conductive laminate sheet (14) attached to said oppositely facing surfaces, respectively, and least one conductive circuit pattern (22) on at least one of said thin rigidifying non-conductive sheets and a plurality of vias (58) thereon [claim 11] including a plurality of vias (58) made by plating build-up (28) and connecting to the core from both the top and bottom sides thereof [claim 12], including a plurality of vias (58) selected from Type 1, Type 2, or Type 3 vias as defined herein [claims 15, 16].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 13, 14, and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over DiStefano in view of US 5,247,246 (Van Loan).

DiStefano discloses the claimed invention including that the conductive metal core layer is copper (see col. 14, lines 50-60) and that the laminate sheets are fiberglass (see col. 14, lines 35-50). DiStefano does not specifically state that the copper layer is in the range of 5-15 mils thick [claim 13]. However, it is well known in

the art to comprise conductive copper layer of a thickness in the range of 5-15 mils as evidenced by Van Loan (see col. 12, lines 35-40). Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the copper layer in the invention of DiStefano with a thickness in the range of 5-15 mils as is known in the art and evidenced by Van Loan. The motivation for doing so would have been to provide a layer of copper with a thickness sufficient for electrical conduction yet thin enough to not adversely effect the overall height of the device. Moreover, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering that optimum or workable ranges involves only routing skill in the art. *In re Aller,* 105 USPQ 233. Additionally, the modified invention of DiStefano teaches one or more additional non-conductive and conductive layers thereon (see figure 3) [claim 14].

Similarly, DiStefano discloses, a thermally enhanced printed circuit (PC) wiring board for mounting grid integrated circuit packages thereon (see col. 1, lines 35-45) comprising a conductive metal core layer (30) having oppositely facing surfaces and one or more holes (58) in the metal core at each of plurality of through-core via sites, a first and second thin rigidifying non-conductive laminate sheet (14) attached to said oppositely facing surfaces, respectively, at least one conductive circuit pattern (22) on at least one of said thin rigidifying non-conductive sheets and a plurality of vias (58) selected from Type 1, Type 2, or Type 3 vias made by plating build-up (28) and connecting to the core from both the top and bottom sides thereof, respectively. DiStefano does not specifically state that the copper layer is in the range of 5-15 mils

thick [claim 17]. However, it is well known in the art to comprise conductive copper layer of a thickness in the range of 5-15 mils as evidenced by Van Loan (see col. 12, lines 35-40). Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the copper layer in the invention of DiStefano with a thickness in the range of 5-15 mils as is known in the art and evidenced by Van Loan. The motivation for doing so would have been to provide a layer of copper with a thickness sufficient for electrical conduction yet thin enough to not adversely effect the overall height of the device. Moreover, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering that optimum or workable ranges involves only routing skill in the art. *In re Aller,* 105 USPQ 233.

Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over DiStefano in view of Van Loan and Frankeny.

DiStefano discloses, a thermally enhanced printed circuit (PC) wiring board and at least one integrated circuit package mounted thereon (see col. 1, lines 35-45) said PC wiring board comprising: a comprising a conductive metal core layer (30) having oppositely facing surfaces and one or more holes (58) in the metal core at each of plurality of through-core via sites, a first and second thin rigidifying non-conductive fiberglass (see col. 14, lines 45-55) laminate sheets (14) attached to said oppositely facing surfaces, respectively, at least one conductive circuit pattern (22) on at least one of said thin rigidifying non-conductive sheets and a plurality of vias (58) selected from Type 1, Type 2, or Type 3 vias made by plating build-up (28) and connecting to the core

from both the top and bottom sides thereof, respectively. DiStefano does not specifically state that the copper layer is in the range of 5-15 mils thick. However, it is well known in the art to comprise conductive copper layer of a thickness in the range of 5-15 mils as evidenced by Van Loan (see col. 12, lines 35-40). Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the copper layer in the invention of DiStefano with a thickness in the range of 5-15 mils as is known in the art and evidenced by Van Loan. The motivation for doing so would have been to provide a layer of copper with a thickness sufficient for electrical conduction yet thin enough to not adversely effect the overall height of the device. Moreover, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering that optimum or workable ranges involves only routing skill in the art. *In re Aller,* 105 USPQ 233. Additionally, the modified invention of DiStefano does not specifically teach that the integrated circuit package is a ball grid integrated circuit package [claim 18]. However, it is well known in the art to comprise integrated circuit packages to be of the ball grid type as evidenced by Frankeny (see col. 7, lines 1-5). Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to use a ball grid integrated circuit package as the integrated circuit package in the modified invention of DiStefano. The motivation for doing so would have been to use an integrated circuit package with a reliable method of electromechanical connection.

Response to Arguments

Applicant's arguments with respect to claims 11-18 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. US 6,204,453, granted to Fallon et al., discloses a PCB with a metal core layer.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeremy C. Norris whose telephone number is 571-272-1932. The examiner can normally be reached on Monday - Friday, 9:30 am - 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JCSN

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